Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (currently amended) A signal processing apparatus comprising:

a source of a fixed rate digital signal;

a signal processor responsive to a burst clock, said signal processor operating in a synchronous-sampling mode for producing a control signal representing a symbol rate; and

an interpolator responsive to the control signal for processing the fixed rate digital signal to yield samples at the symbol rate, said interpolator being further operative to enable a burst clock in response to said samples at the symbol rate being ready to be processed by said signal processor.

2. (original) The signal processing apparatus of claim 1 wherein the interpolator processes the fixed rate digital signal to yield samples at the symbol rate by calculating a symbol value at a symbol location by interpolating a number of fixed rate samples adjacent to the symbol location.

3. (original) The signal processing apparatus of claim 1 wherein the source of the fixed rate digital signal is an analog to digital converter.

4. (original) The signal processing apparatus of claim 1 wherein the interpolator is a cubic interpolator.

5. (original) The signal processing apparatus of claim 1 wherein the interpolator is a linear interpolator.

6. (original) The signal processing apparatus of claim 1 wherein the interpolator is a piecewise parabolic interpolator.

7. (original) The signal processing apparatus of claim 1 wherein the interpolator is internal to an integrated circuit.

8. (original) The signal processing apparatus of claim 1 wherein the interpolator is implemented using software.

9. (currently amended) A method of signal processing comprising the steps of:

receiving a plurality of digital values at a fixed rate of time;

receiving a control signal from a signal processor operating in a synchronous-sampling mode, said signal processor being responsive to a burst clock; ~~and~~ calculating a signal level by interpolating the signal level from the plurality of digital values; and

enabling a burst clock in response to said calculated signal level being available to said signal processor.

10. (original) The method of claim 9 wherein the control signal from the signal processor is a symbol rate.

11. (original) The method of claim 9 wherein the source of the plurality of digital values at a fixed rate of time is an analog to digital converter.

12. (original) The method of claim 9 wherein the step of calculating a signal level by interpolating the signal level from the plurality of digital values is preformed using a cubic interpolator.

13. (original) The method of claim 9 wherein the step of calculating a signal level by interpolating the signal level from the plurality of digital values is preformed using a linear interpolator.

14. (original) The method of claim 9 wherein the step of calculating a signal level by interpolating the signal level from the plurality of digital values is preformed using a piecewise parabolic interpolator.

15. (currently amended) A signal processing apparatus comprising:

a source of an analog signal;

an analog to digital converter for converting the analog signal to a fixed rate digital signal;

a demodulator operating in a synchronous-sampling mode;

a processor responsive to a burst clock, said processor operative for producing a control signal representing a symbol rate; and

an interpolator responsive to the control signal for processing the fixed rate digital signal to yield samples at the symbol rate by calculating a symbol value at a symbol location by interpolating a number of fixed rate samples adjacent to said symbol location and outputting the samples to the demodulator, said interpolator being further operative to enable a burst clock in response to said samples at the symbol rate being ready to be processed by said signal processor.

16. (original) The signal processing apparatus of claim 15 wherein the interpolator is a cubic interpolator.

17. (original) The signal processing apparatus of claim 15 wherein the interpolator is a linear interpolator.

18. (original) The signal processing apparatus of claim 15 wherein the interpolator is a piecewise parabolic interpolator.

19. (original) The signal processing apparatus of claim 15 wherein the interpolator is internal to an integrated circuit.

20. (original) The signal processing apparatus of claim 15 wherein the interpolator is implemented using software.